Claims

The claims are amended as follows:

1. (Currently Amended) An image sensor using correlated double sampling technology which outputs data of an object by using difference between a reset voltage signal and a data voltage signal of a unit pixel, comprising:

a plurality of unit pixels arranged in a matrix, each outputting the reset voltage signal and the data voltage signal;

a plurality of clamping means, each coupled to each unit pixels for clamping up the reset signal to a predetermined voltage level; and

a voltage controlling block for adjusting voltage level supplied to a gate of each of clamping means, wherein the voltage controlling block include: a D/A converting means for receiving a digital code and outputting an analog voltage used to adjust the voltage level;

a first switch coupled between the D/A converting means and the clamping means and controlled by a first control signal; and

a second switch coupled between a ground voltage and the clamping means and controlled by an inverse of the first control signal.

2. (Canceled)

3. (Original) The image sensor as recited in claim 2, wherein the voltage controlling block includes an inverter, connected to the second switch, for inverting the first control signal.

4. (Original) The image sensor as recited in claim 2, wherein each clamping means is composed of one MOS transistor coupled between supply voltage and an output node of each pixel.

5. (Original) The image sensor as recited in claim 4, wherein the first switch is coupled to a gate of the MOS transistor of clamping means.

6. (Original) The image sensor as recited in claim 1 , wherein each clamping means is included in each column of the matrix and one voltage controlling block is in whole chip of one image sensor.

7. (Currently Amended) An image sensor using correlated double sampling technology which outputs data of an object by using difference between a reset voltage signal and a data voltage signal of a unit pixel, comprising:

a plurality of unit pixels arranged in a matrix, each outputting the reset voltage signal and the data voltage signal;

a plurality of ~~clamping unit~~clamping units, each coupled to ~~each~~ one of the unit pixels for clamping up the reset signal to a predetermined voltage level; and

a voltage controlling block for adjusting voltage level supplied to a gate of each ~~of~~ clamping unit,

wherein the voltage controlling block includes:

a D/A converter for receiving a digital code and outputting an analog voltage used to adjust the voltage level;

a first switch coupled between the D/A converter and one of the clamping units and controlled by a first control signal; and

a second switch coupled between a ground voltage and said one of the clamping units and controlled by an inverse of the first control signal.

8. (Canceled)

9. (Previously Presented) The image sensor as recited in claim 8, wherein the voltage controlling block Includes an inverter, connected to the second switch, for inverting the first control signal.

10. (Previously Presented) The image sensor as recited in claim 8, wherein each clamping unit is composed of one MOS transistor coupled between supply voltage and an output node of each pixel.

11 . (Previously Presented) The image sensor as recited in claim 10, wherein
the first switch is coupled to a gate of the MOS transistor of clamping unit.

12. (Previously Presented) The image sensor as recited in claim 7, wherein each clamping unit is included in each column of the matrix and one voltage controlling block is in whole chip of one image sensor.